

## CLAIMS

1-26. (canceled)

27. (new) In a system comprising a first processor and one or more other processors, a method for applying one or more interrupt signals to the one or more other processors, the method comprising:

- (a) generating, in the first processor, a data signal having one or more data bits;
- (b) transmitting the data signal from a data port of the first processor to a signal unit external to the first processor and the one or more other processors;
- (c) converting, in the signal unit, the data signal into one or more interrupt signals, wherein each data bit in the data signal corresponds to a different interrupt signal; and
- (d) transmitting each interrupt signal from the signal unit to an interrupt port of an other processor.

28. (new) The invention of claim 27, wherein:  
the data signal has a plurality of data bits;  
the signal unit converts the data signal into a plurality of interrupt signals; and  
each interrupt signal is transmitted to a different interrupt port of an other processor.

29. (new) The invention of claim 28, wherein at least two interrupt signals are transmitted to two different interrupt ports of a single other processor.

30. (new) The invention of claim 28, wherein at least two interrupt signals are transmitted to interrupt ports of at least two different other processors.

31. (new) The invention of claim 27, wherein the signal unit detects a transition in each data bit of the data signal over time to determine when to generate a corresponding interrupt signal.

32. (new) The invention of claim 31, wherein the signal unit detects the transition by:  
storing sequential values for the corresponding data bit in two registers; and  
comparing outputs from the two registers to detect a difference between the two sequential values.

33. (new) The invention of claim 32, wherein:  
the first processor transmits an address signal to the signal unit; and  
the signal unit compares the address signal to a specified value to determine whether to store the two sequential values in the two registers.

34. (new) The invention of claim 27, wherein each interrupt signal is transmitted from the signal unit to a corresponding interrupt port of a corresponding other processor via a dedicated line.

35. (new) The invention of claim 34, wherein the data signal is transmitted from the first processor to the signal unit via a shared data bus.

36. (new) The invention of claim 27, further comprising applying an interrupt signal from an other processor to the first processor by:

- (1) generating, in the other processor, an other data signal having one or more other data bits;

5 (2) transmitting the other data signal from a data port of the other processor to an other  
6 signal unit external to the first processor and the one or more other processors;  
7 (3) converting, in the other signal unit, the other data signal into one or more other interrupt  
8 signals, wherein each other data bit in the other data signal corresponds to a different other interrupt  
9 signal; and  
10 (4) transmitting an other interrupt signal from the other signal unit to an interrupt port of the  
11 first processor.

1 37. (new) The invention of claim 36, wherein at least one other interrupt signal is  
2 transmitted from the other signal unit to an interrupt port of at least one other processor.

1 38. (new) A system comprising a first processor connected to one or more other processors  
2 via a signal unit external to the first processor and the one or more other processors, wherein:  
3 the first processor is adapted to (i) generate a data signal having one or more data bits and (ii)  
4 transmit the data signal from a data port of the first processor to the signal unit; and  
5 the signal unit is adapted to (i) convert the data signal into one or more interrupt signals, wherein  
6 each data bit in the data signal corresponds to a different interrupt signal, and (ii) transmit each interrupt  
7 signal from the signal unit to an interrupt port of an other processor.

1 39. (new) The invention of claim 38, wherein:  
2 the data signal has a plurality of data bits;  
3 the signal unit is adapted to convert the data signal into a plurality of interrupt signals; and  
4 the signal unit is connected to transmit each interrupt signal to a different interrupt port of an  
5 other processor.

1 40. (new) The invention of claim 39, wherein the signal unit is connected to transmit at least  
2 two interrupt signals to two different interrupt ports of a single other processor.

1 41. (new) The invention of claim 39, wherein the signal unit is connected to transmit at least  
2 two interrupt signals to interrupt ports of at least two different other processors.

1 42. (new) The invention of claim 38, wherein the signal unit is adapted to detect a transition  
2 in each data bit of the data signal over time to determine when to generate a corresponding interrupt  
3 signal.

1 43. (new) The invention of claim 42, wherein the signal unit comprises:  
2 two registers adapted to store sequential values for each data bit; and  
3 logic adapted to compare outputs from the two registers to detect the transition for a  
4 corresponding data bit as a difference between the two sequential values.

1 44. (new) The invention of claim 43, wherein:  
2 the first processor is adapted to transmit an address signal to the signal unit; and  
3 the signal unit comprises an address decoder adapted to compare the address signal to a specified  
4 value to determine whether to store the two sequential values in the two registers.

1 45. (new) The invention of claim 38, wherein the signal unit is connected to transmit each  
2 interrupt signal to a corresponding interrupt port of a corresponding other processor via a dedicated line.

1 46. (new) The invention of claim 45, wherein the first processor is connected to transmit the  
2 data signal to the signal unit via a shared data bus.

1           47.     (new) The invention of claim 38, further comprising an other signal unit connecting an  
2 other processor to the first processor, wherein:  
3           the other signal unit is external to the first processor and the one or more other processors;  
4           the other processor is adapted to (i) generate an other data signal having one or more other data  
5 bits and (ii) transmit the other data signal from a data port of the other processor to the other signal unit;  
6 and  
7           the other signal unit is adapted to (i) convert the other data signal into one or more other interrupt  
8 signals, wherein each other data bit in the other data signal corresponds to a different other interrupt  
9 signal and (ii) transmit an other interrupt signal from the other signal unit to an interrupt port of the first  
10 processor.

1           48.     (new) The invention of claim 47, the other signal unit is adapted to transmit at least one  
2 other interrupt signal to an interrupt port of at least one other processor.

1           49.     (new) A first processor for a system comprising the first processor connected to one or  
2 more other processors via a signal unit external to the first processor and the one or more other  
3 processors, wherein:  
4           the first processor is adapted to (i) generate a data signal having one or more data bits and (ii)  
5 transmit the data signal from a data port of the first processor to the signal unit; and  
6           the signal unit is adapted to (i) convert the data signal into one or more interrupt signals, wherein  
7 each data bit in the data signal corresponds to a different interrupt signal, and (ii) transmit each interrupt  
8 signal from the signal unit to an interrupt port of an other processor.

1           50.     (new) The invention of claim 49, wherein the first processor is adapted to transmit the  
2 data signal to the signal unit via a shared data bus.

1           51.     (new) A signal unit for a system comprising a first processor connected to one or more  
2 other processors via the signal unit external to the first processor and the one or more other processors,  
3 wherein:  
4           the first processor is adapted to (i) generate a data signal having one or more data bits and (ii)  
5 transmit the data signal from a data port of the first processor to the signal unit; and  
6           the signal unit is adapted to (i) convert the data signal into one or more interrupt signals, wherein  
7 each data bit in the data signal corresponds to a different interrupt signal, and (ii) transmit each interrupt  
8 signal from the signal unit to an interrupt port of an other processor.

1           52.     (new) The invention of claim 51, wherein:  
2           the data signal has a plurality of data bits;  
3           the signal unit is adapted to convert the data signal into a plurality of interrupt signals; and  
4           the signal unit is adapted to transmit each interrupt signal to a different interrupt port of an other  
5 processor;  
6           the signal unit is adapted to transmit at least two interrupt signals to two different interrupt ports  
7 of a single other processor;  
8           the signal unit is adapted to transmit at least two interrupt signals to interrupt ports of at least two  
9 different other processors;  
10          the signal unit is adapted to detect a transition in each data bit of the data signal over time to  
11 determine when to generate a corresponding interrupt signal;  
12          the signal unit is adapted to receive the data signal from the first processor via a shared data bus;  
13 and  
14          the signal unit is adapted to transmit each interrupt signal to a corresponding interrupt port of a  
15 corresponding other processor via a dedicated line.